(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 392 565 A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: 90107265.2

(51) Int. Cl.5: G06F 13/42

(22) Date of filing: 17.04.90

(30) Priority: 14.04.89 JP 96080/89

(43) Date of publication of application:
17.10.90 Bulletin 90/42

(84) Designated Contracting States:
DE FR GB

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## (54) System bus control system.

(57) A system bus control system for controlling the data transmission between a master system and a plurality of slave systems coupled to the master system through system buses, wherein the master system sends to the slave systems first strobe signals representing the data transferring timing and second strobe signals delayed by a predetermined period of time which corresponds to the accessing time, on the other hand, the slave systems output replying signal to the master system when the slave systems receive the first strobe signal and in turn receiving the second strobe signal, the slave system sends the replying signal to the master system.

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# SYSTEM BUS CONTROL SYSTEM

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a system bus control system used for controlling the data transferring between a master system and slave system connected by a multi bus or a VME bus.

### Description of the Prior Art

Conventionally, as a system bus control system of the above type, there has been known such a system that a master system sends a series of data transferring strobe signals for designating the data transferring timing corresponding to respective slave systems. Upon receipt of the data transferring strobe signal corresponding to the slave systems respectively, the slave system which has received the corresponding strobe signal starts count an accessing time, and after the accessing time has been counted, a data transferring replying signal is outputted from the slave system to the master system.

Figs. 1 and 2 show the read timing and write timing of the multi bus employed in the conventional system bus control system mentioned above. Figs. 3 and 4 show the timing in a i bite read cycle and the timing in a 1 bite write cycle of the VME bus employed in the conventional system bus control system.

The data transferring strobe signals are shown by MRDC* and IORC* in Fig. 1, MWTC* and IOWC* in Fig. 2 and DS0* and DS1* in Figs. 3 and 4. The data transferring and replying signals are shown by XACK* in Figs, 1 and 2, DTACK* and BERR* in Figs. 3 and 4. In Figs. 3 and 4, IACK*shows interrupt acknowledge signal, A01 to A31, AM0* to AM5 and LWORD* show address data, AS* shows an address strobe signal representing the decision of the address, WRITE* shows read/write signal and D00 to D07 show the transferring data.

When the master system outputs the data transferring strobe signal to the slave systems and the corresponding data transferring strobe signal is received by the slave system, which outputs the data transfer and replying signal to the master system after the data accessing time has been counted.

Fig. 5 shows an example of a conventional circuit arrangement of a data transferring and replying signal unit used in the slave system of the access time of 200 nano seconds.. The data transferring and replying signal unit comprises a 10MHz clock generator 111, a shift register 113 having three flip-flops 112, an OR gate 114, an AND gate 116, a tri-state output gate 116 and a decode circuit 117. In the circuit arrangement mentioned above, when the data transferring strobe signal MRDC* or IORC* sown in Fig. 1 becomes active, or the data transferring strobe signal MWTC* or IOWC* in Flg. 2 becomes active, the time counting is started and the time corresponding to the accessing time has been counted, the data transferring and replying signal XACK* is outputted.

In the conventional system bus control system, it is necessary to provide a circuit arrangement including a set of the shift registers or a counter for counting the accessing time, therefore, there is such a problem that the circuit arrangement of the slave system is much complicated.

## SUMMARY OF THE INVENTION

An essential object of the present invention is to provide a system bus control system in which the slave system does not require to provide any shift register or counter for counting the accessing time.

In order to accomplish the object of the present invention, there is provided a system bus control system for controlling the data transmission between a master system and a plurality of slave systems coupled to the master system through system buses, wherein the master system sends to the slave systems first strobe signals representing the data transferring timing and second strobe signals delayed by a predetermined period of time which corresponds to the accessing time, on the other hand, the slave systems output replying signal to the master system when the slave systems receive the first strobe signal and in turn receiving the second strobe signal, the slave system sends the replying signal to the master system.

In operation, the master system sends to the respective slave systems the first strobe signals representing the data transferring timing and the second strobe signal delayed by a predetermined period of time which corresponds to the accessing time from the first strobe signal. On the other hand, when the slave system output replying signal to the master system when the slave system receives the second strobe signal after receipt of the first strobe signal, the slave system sends the data transfer and replying signal to the master system. Therefore, there is no need to provide any counter or shift registers in the slave system for counting the

accessing time.

## BRIEF EXPLANATION OF THE DRAWINGS

Fig. 1 is a time chart for showing the write timing in the multi bus of the conventional system bus control system,

Fig. 2 is a time chart for showing the read timing in the multi bus of the conventional system bus control system,

Fig. 3 is a time chart for showing the timing in the VME bus in the read cycle in an example of a prior art,

Fig. 4 is a time chart for showing the timing in the VME bus in the write cycle in the prior art,

Fig. 5 is a circuit diagram of a conventional data transferring and replying unit,

Fig. 6 is a time chart for showing the read timing in an example of the system bus control system according to the present invention,

Fig. 7 is a time chart for showing the write timing in the example,

Fig. 8 is a circuit diagram of an embodiment of a strobe signal generating circuit for performing the example shown in Figs. 6 and 7,

Fig. 9 is a state shift chart of the strobe signal in the above mentioned example.

Fig. 10 is a circuit diagram showing an example of the data transferring and replying unit,

Fig. 11 is a time chart for showing the data read timing in the case where the data transferring and replying unit shown in Fig. 10 is used, and

Fig. 12 is a block diagram showing relation between the master system and the slave system.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 6, the master system sends the address data to an address bus (not shown) and after the address data is stabilized, the master system makes the strobe signal STB1* acitve. Further the master system makes the respective strobe signals STB2*, STB3*, ... STBn* active sequentially one by one in the written order with a predetermined time period, for example, every 100 nano seconds. The last strobe signal STBn* is activated after such a time period that the access time of the slave system is passed from the activating time of STB1*. When the slave system receives the strobe signal STB1*, thereby outputting the data to the data bus. When the slave system receives the strobe signal STBn*, an answering signal RDY* is activated. Receiving the answering signal RDY*, the master system reads the data on the data bus and makes all of the strobe signals STB1* to STBn* non active. Thereafter the master system stops output the address data. When the signal STB1* becomes non active, the slave system stops output the data to the data bus, making the signal "RDY*" non active.

In Fig. 7, the master system writes the data which is already outputted to the data bus in the slave system after the signal RDY* is turned to active. Other operations are the same as shown in Fig. 6.

Usually most of the access time of the slave system such as an I/O device or a memory is less than 300 nano seconds, therefore, if the time difference of the adjacent strobe signals is 100 nano seconds, it is sufficient to provide four strobe signals.

Fig. 8 shows a strobe signal generator for generating three strobe signals. The circuit shown in Fig. 8 comprises three OR gates 31, four AND gates 32 and three flip flops 33. With the bus use start signal "start" and clock signals $\phi$, the respective strobe signals STB1*, STB2* AND STB3* are sequentially activated in the order as described on at one time. When RDY* is activated, the strobe signals mentioned above are inactivated.

Fig. 9 shows state shifts of the circuit shown in Fig. 8. The states of the strobe signals [STB1*, STB2* and STB3*] are [1, 1, 1] when the signal START = 0. When the signal START = 1, the state changes to [0, 1, 1]. When the START is non active, that is RDY* = 1, the strobe signal changes from [0, 0, 1] to [0, 0, 0]. In the course of the state shift as mentioned above, if the signal RDY* becomes 0, the original state 1, 1, 1 can be restored.

Fig. 10 shows a circuit diagram of a data transferring and replying unit of a slave system having access time of 200 nano seconds and connected to a system bus which is operated with strobe signals having a time difference of 100 nano seconds and Fig. 11 shows its data reading timing. This circuit is composed of an AND gate 51, a tri-state output gate 52 and a decode circuit 53. When the strobe signal STB1* becomes active, the output of the tri-state output gate 52 becomes not high impedance (Hi-Z) condition and outputs the signal "RDY*" of non active. Upon receipt of the signal "STB3*", the signal "RDY*" is made active.

As shown in Fig. 10, the circuit arrangement of the data transferring and replying unit becomes remarkably simple compared to the conventional data transferring and replying unit as shown in Fig. 5.

As described above, according to the system bus control system of the present invention, since it is unnecessary to provide any shift register or counter for counting the accessing time in the slave system, the configuration of the slave system can be simplified.

## Claims

1. A system bus control system for controlling the data transmission between a master system and a plurality of slave systems coupled to the master system through system buses, wherein the master system sends to the slave systems first strobe signals representing the data transferring timing and second strobe signals delayed by a predetermined period of time which corresponds to the accessing time, on the other hand, the slave systems output replying signal to the master system when the slave systems receive the first strobe signal and in turn receiving the second strobe signal, the slave system sends the replying signal to the master system.

Fig. 1

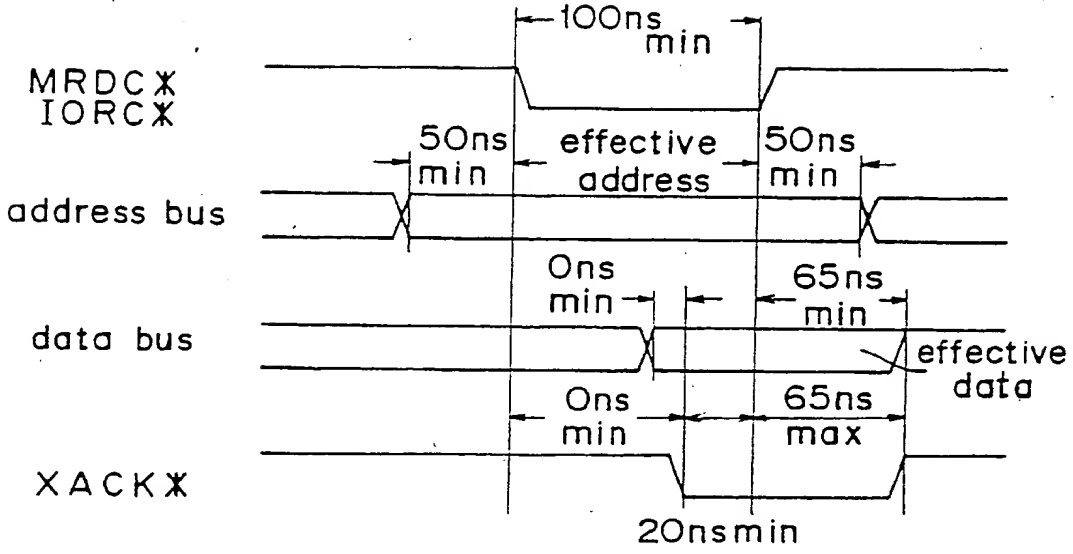

100ns min
MRDC*
IORC*
50ns min
effective address
50ns min
address bus
0ns min
65ns min
data bus
effective data
0ns min
65ns max
XACK*
20ns min

Fig. 2

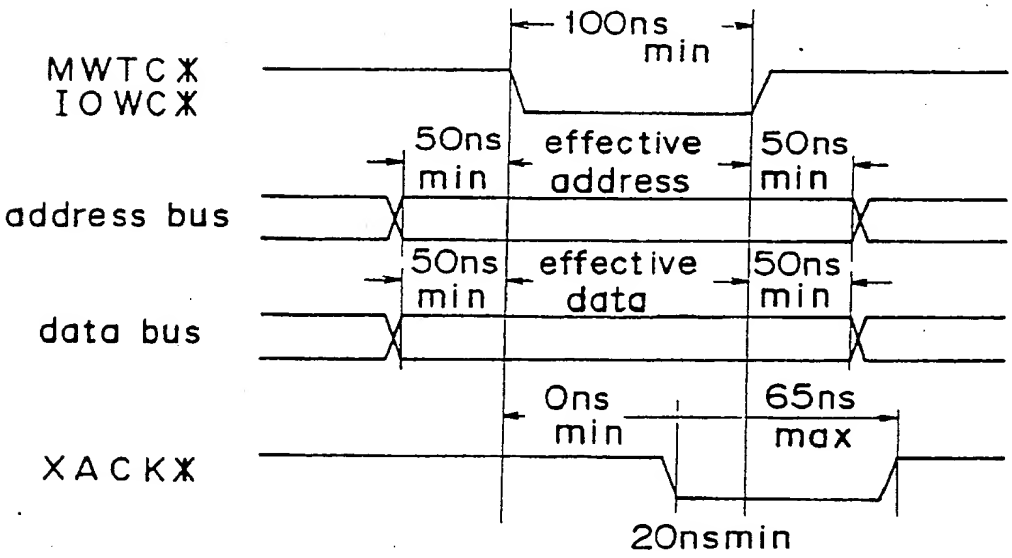

100ns min
MWTC*
IOWC*
50ns min
effective address
50ns min
address bus
50ns min
effective data
50ns min
data bus
0ns min
65ns max
XACK*
20ns min

Fig . 3

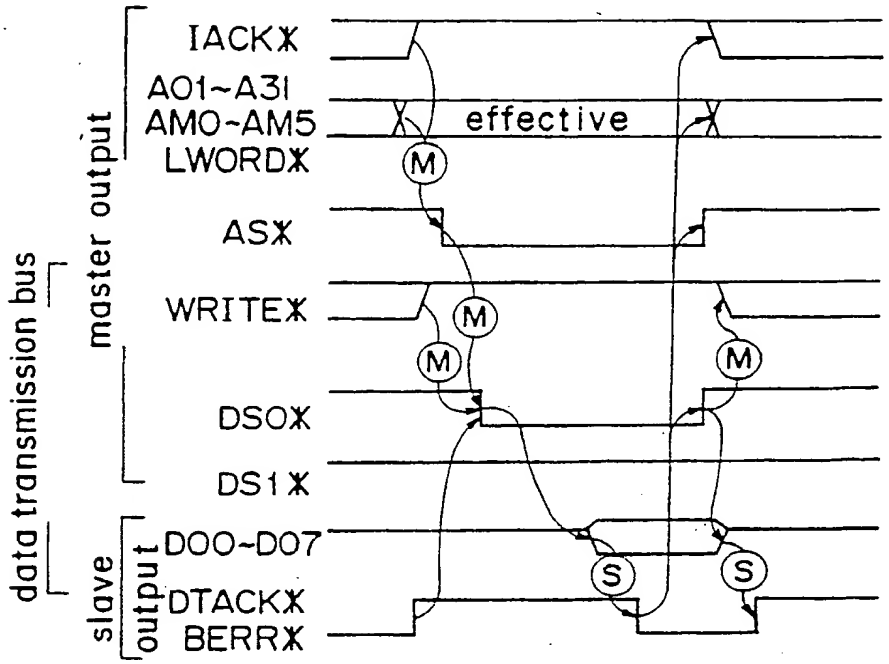

data transmission bus
master output
slave output
IACKX
A01~A31
AM0~AM5
LWORDX
ASX
WRITEX
DSOX
DS1X
DOO~D07
DTACKX
BERRX
effective
M
S

Fig . 4

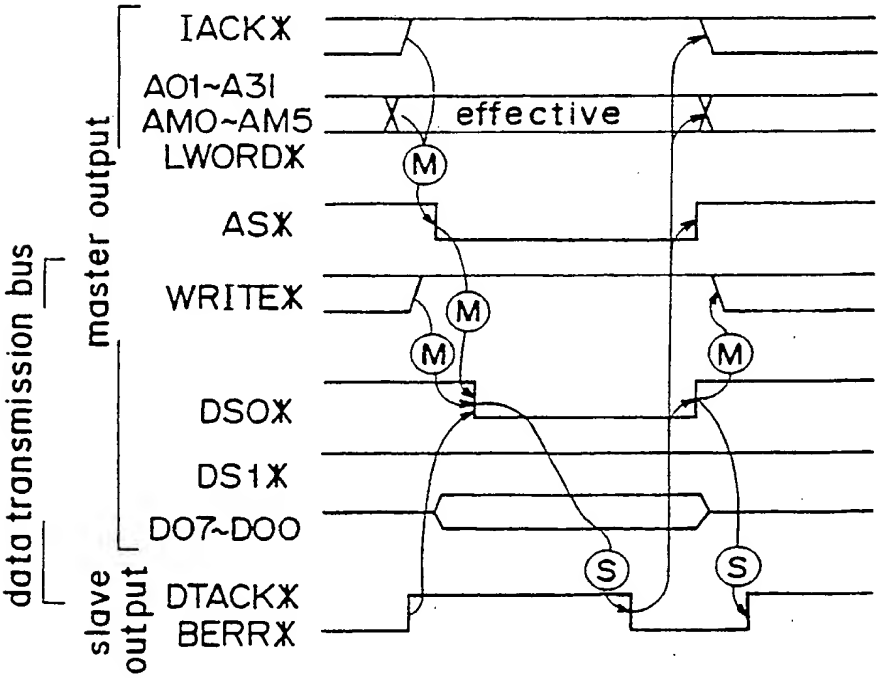

data transmission bus
master output
slave output
IACKX
A01~A31
AM0~AM5
LWORDX
ASX
WRITEX
DSOX
DS1X
DO7~DOO
DTACKX
BERRX
effective
M
S

Fig. 5

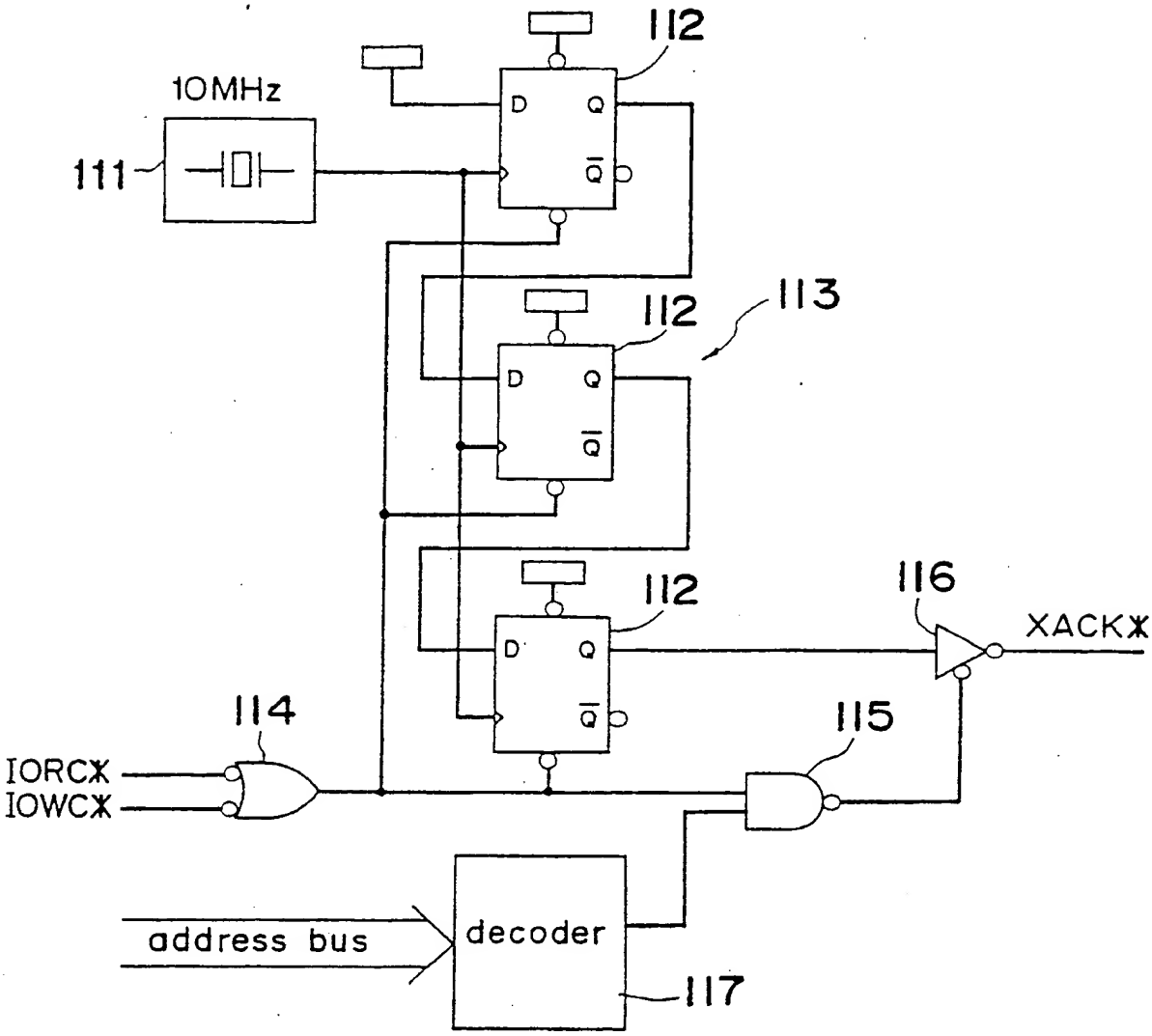

10MHz
111
112
D
Q
Q̄
112
113
D
Q
Q̄
112
116
XACKX
D
Q
Q̄
114
IORCX
IOWCX
115
address bus
decoder
117

Fig . 6

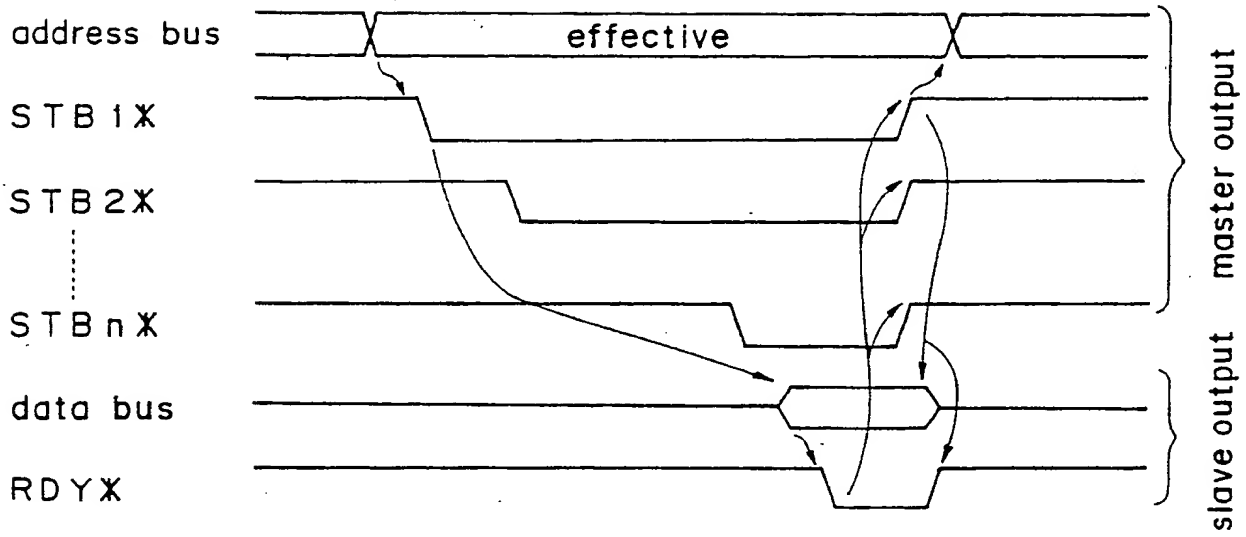

address bus
effective
STB 1*
STB 2*
STB n*
data bus
RDY*
master output
slave output

Fig . 7

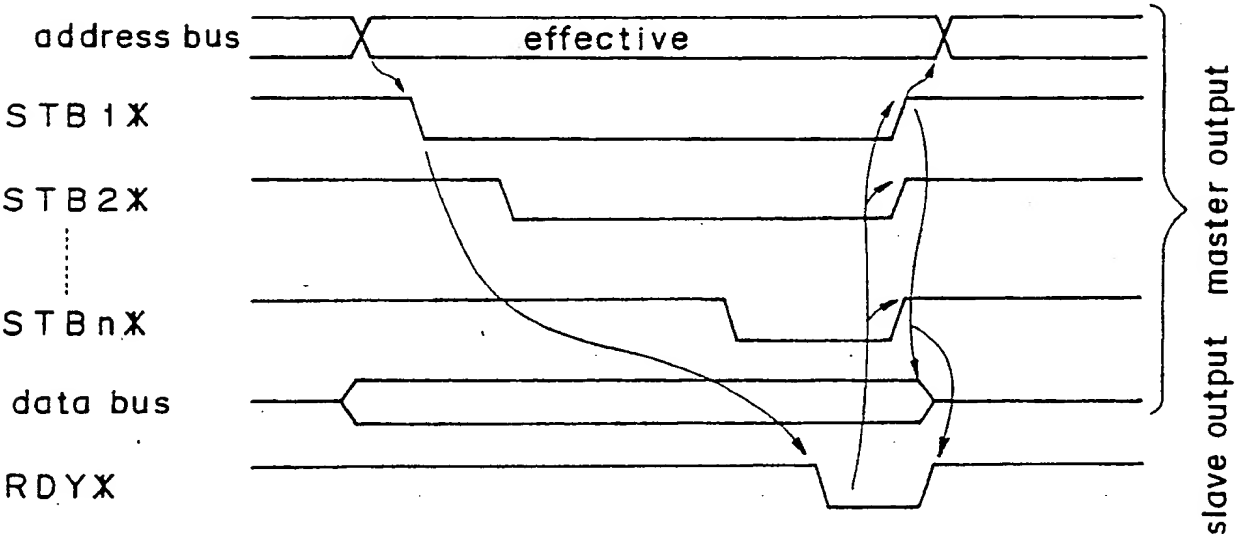

address bus
effective
STB 1*
STB2*
STBn*
data bus
RDY*
master output
slave output

Fig . 8

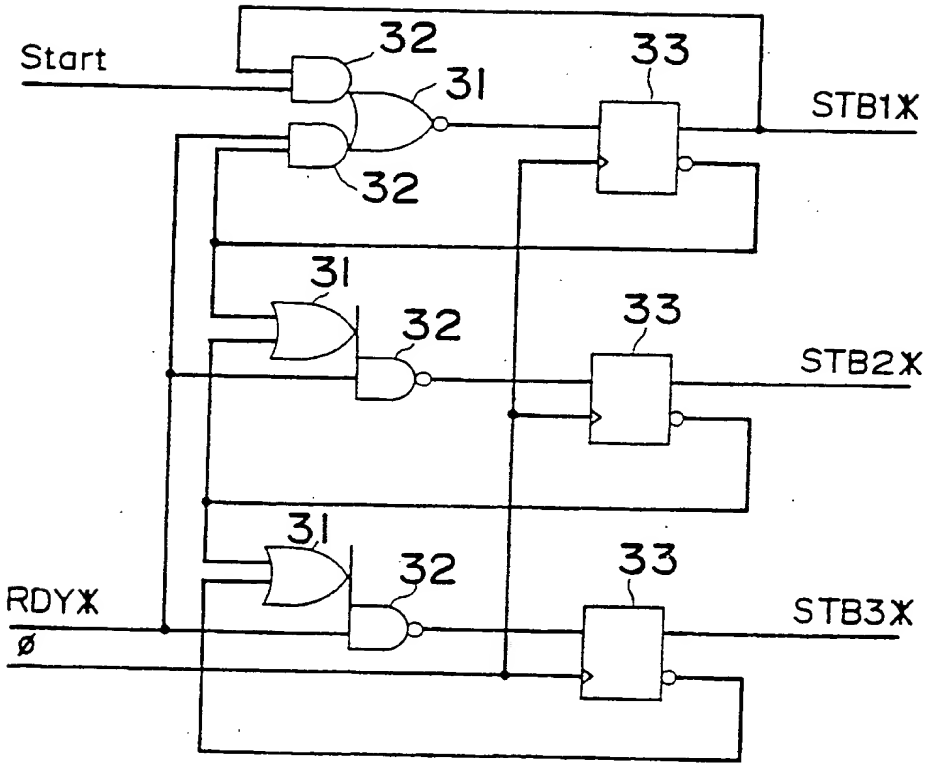


*Fig. 9*

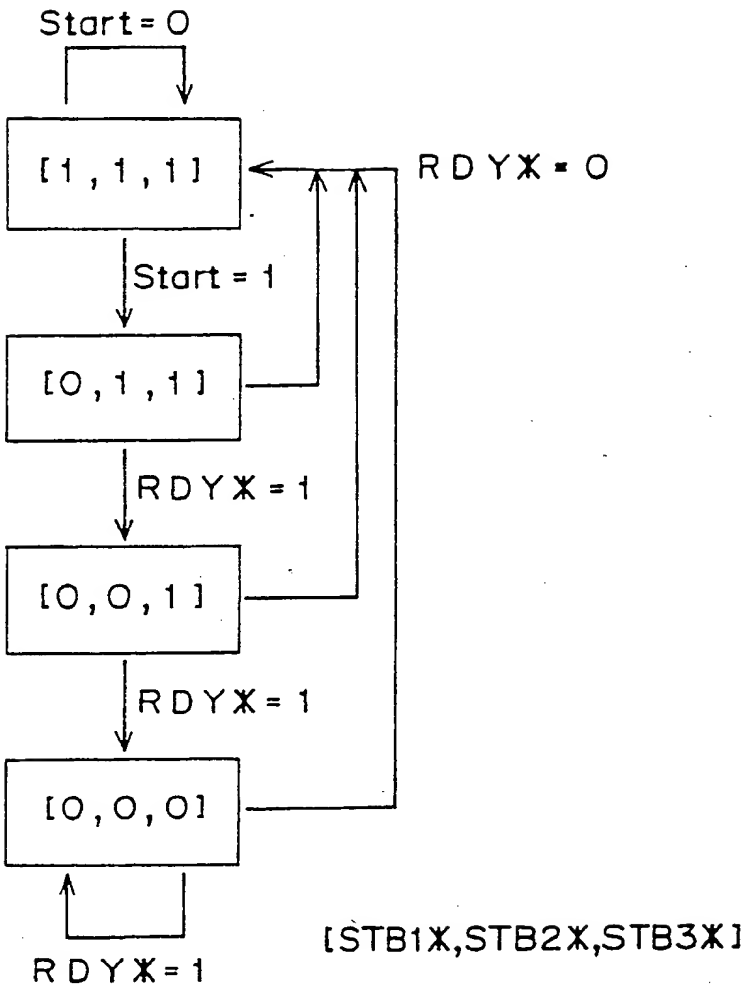

Start = 0
[1, 1, 1]
RDYX = 0
Start = 1
[0, 1, 1]
RDYX = 1
[0, 0, 1]
RDYX = 1
[0, 0, 0]
RDYX = 1
[STB1X, STB2X, STB3X]

Fig. 10

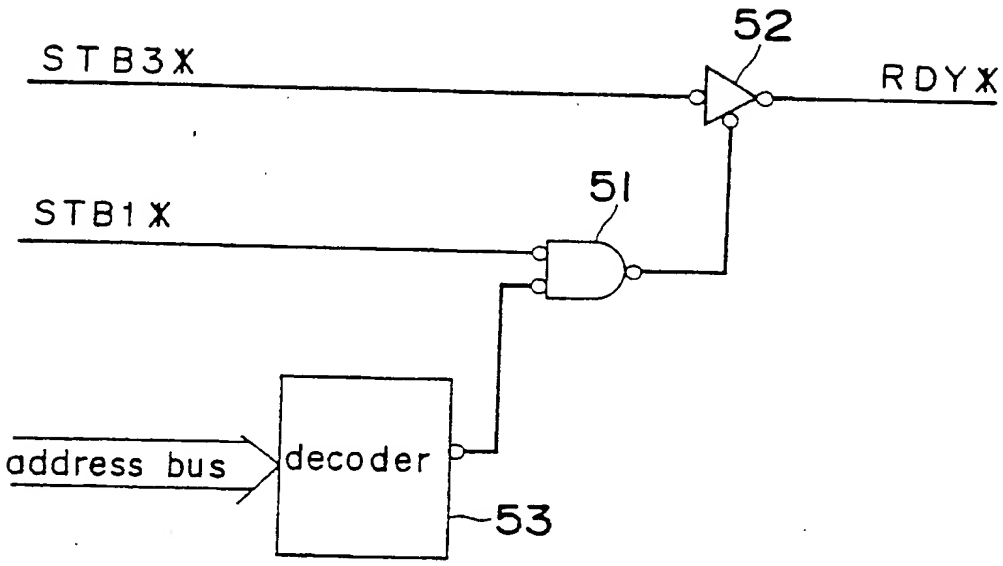
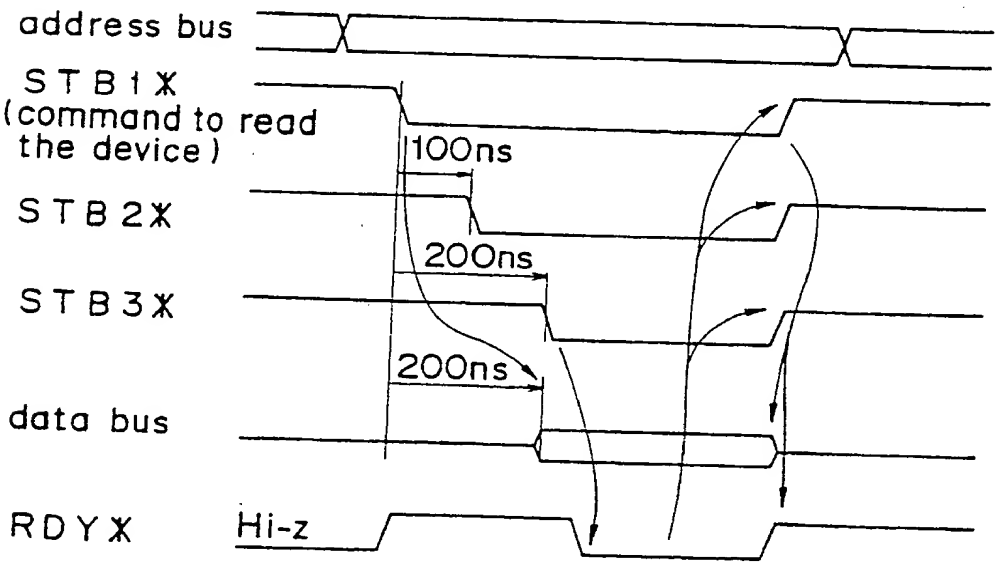



Fig. 11




When the data is read

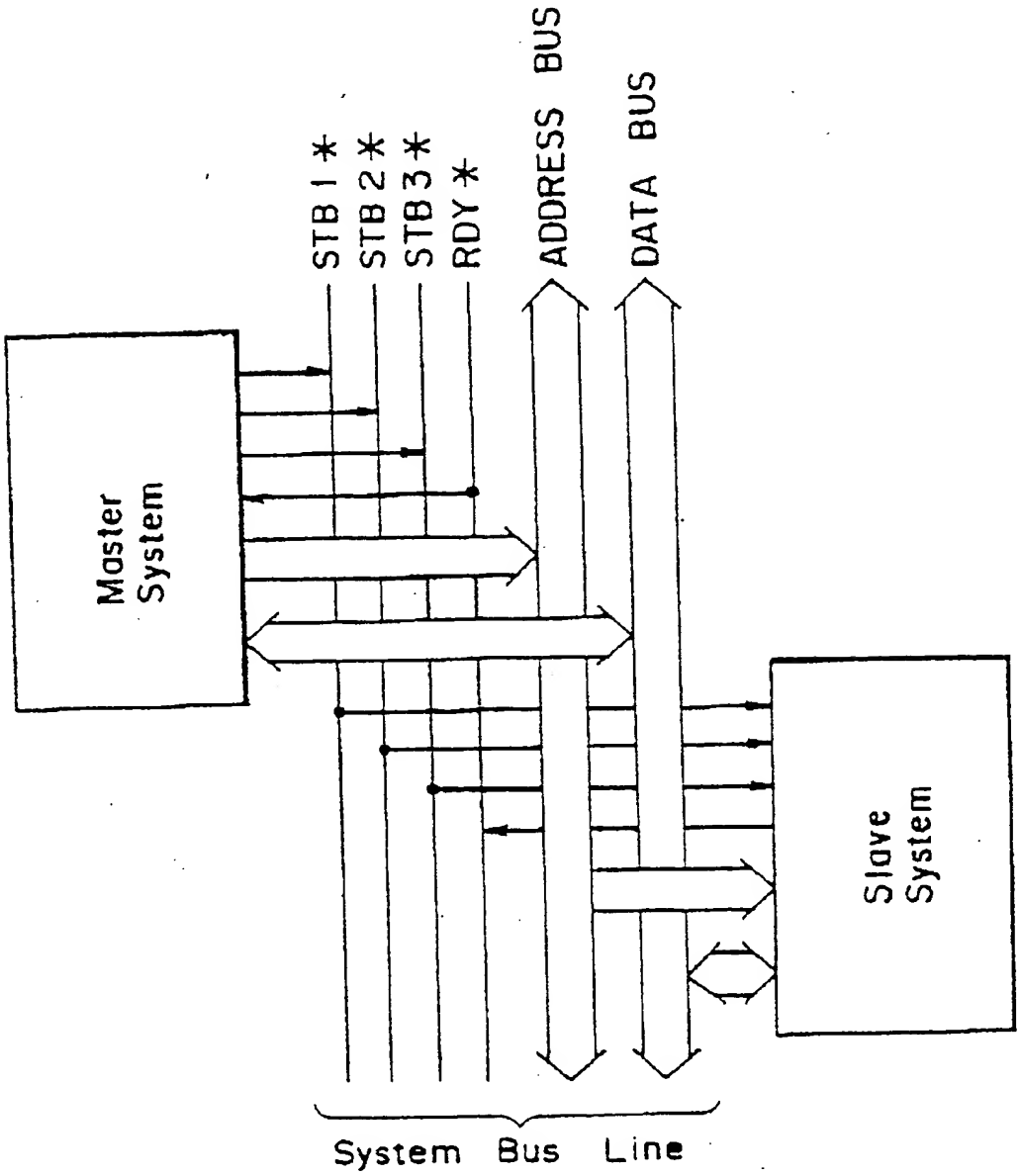

STB 1 *
STB 2 *
STB 3 *
RDY *
ADDRESS BUS
DATA BUS
Master System
Slave System
System Bus Line

Fig. 12

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(11) Publication number: **0 392 565 A3**

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(51) Int. Cl.5: **G06F 13/42**

(22) Date of filing: **17.04.90**

(30) Priority: **14.04.89 JP 96080/89**

(43) Date of publication of application:
**17.10.90 Bulletin 90/42**

(84) Designated Contracting States:
**DE FR GB**

(88) Date of deferred publication of the search report:
**18.09.91 Bulletin 91/38**

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European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 90 10 7265

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | EP-A-0 081 961 (DATA GENERAL CORP.)<br>* Page 2, line 6 - page 3, line 5; page 6, lines 10-21; page 9, line 25 - page 10, line 17; page 19, lines 12-29 * | 1 | G 06 F 13/42 |
| Y | EP-A-0 051 920 (NEC CORP.)<br>* Page 3, lines 6-11; page 4, lines 11-16; page 7, lines 1-10; page 8, line 21 - page 9, line 3; figures 2,6 * | 1 | |
| Y | US-A-4 463 440 (NISHIURA et al.)<br>* Column 1, lines 10-21; column 3, line 37 - column 4, line 14; claim 1; figures 3,4 * | 1 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 06 F 13/42

The present search report has been drawn up for all claims

| Place of search | Date of completion of search | Examiner |
|---|---|---|
| The Hague | 05 July 91 | NGUYEN XUAN HIEP C. |

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document